IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 2, Issue 4, Aug-Sept, 2014
ISSN: 2320 – 8791 (Impact Factor: 1.479)
www.ijreat.org

An Effective Way Of Reducing The Leakage Power By Sleep Methods In Deep Submicron Circuits

Kodali Venkata Bhanu Prakash[1], Ms. M.Pavitra[2]

[1]*PG Student (M.Tech-VLSI), ECE Department, PBR VITS, Kavali, Nellore D.T., A.P., INDIA*

[2]*Associate Professor, ECE Department, PBR VITS, Kavali, Nellore D.T., A.P., INDIA*

Abstract

In CMOS integrated circuit design the higher power consumption is a great challenge due to the voltage scaling as it leads to increase in the sub- threshold leakage current. The major portion of total power consumption is the Leakage power dissipation and it is growing exponentially in the integrated devices. So, the reduction of leakage power is very important for low power applications. This paper enumerates a logic circuitry design with low area and low power. In this paper the existing techniques are compared with the proposed technique and a comparative analysis is done. With the help DSCH (for Schematic Design), and Microwind (for layout and Power Simulation) we compared the simulation for different architectures including existing and proposed architectures.

Key Words: *Sub-threshold Leakage, leakage power, DSCH, Microwind.*

----------***----------

1. INTRODUCTION

For CMOS technology one of the top issues is Power consumption. To achieve high performance and high density, CMOS technology feature size and threshold voltage have been scaling down from a long time. In MOS transistors with deep submicron technology, an undesirable power consumption consequence arises. VDD (Supply voltage) has been scaled down in order to keep the power consumption under control. Hence, the Vth (threshold voltage) has to be proportionately scaled to maintain a high current drive and also to achieve the performance. However, the threshold voltage scaling results in thesturdy increase of the sub-threshold leakage current.

Hence, it has become utmost important to develop design techniques for thereduction of power dissipation. The Components which determines the power consumptionin a CMOS circuit are:

During the transition of signals from1 to 0and from 0 to 1both networks of CMOS circuit's pmos and nmoswill be on for a whilewhich leads to short-circuit power dissipation P_{sc}which is given by the equation

$$P_{sc}=I_{sc}.V_{dd}.t_s.f_{sw}$$

Where $I_{sc}$is the short circuit current, $t_s$is theswitching delay. Both sources of power dissipation (P_{dyn} and P_{sc}) in a CMOS circuitis related totransitions at gate outputs and are thereforecollectively referred to as active dissipation. Incontrast, the third source of power dissipationisdue to leakage current, which flows when theinputs and outputs are changing their state and is called static dissipation (P_{static}).

Static power includes sub-threshold leakage, drainjunction leakage and also the gate leakage. So, In a CMOS circuit, static dissipation is due toleakage current, which is generally small in magnitude and is given by

$$P_{leak}= I_{leak}.V_{dd}$$

Dynamic power (Includes charging, discharging power and short circuit power).The totaldynamic power consumption is given by

$$P_{dynamic} = KCV_{dd}^2f_{sw}$$

Where k is technology factor,
C is thecapacitance of switching nodes,
V_{dd} is the supplyvoltage and
f_{sw} is the effective switchingfrequency.

Theexpression for the total powercomparison is as follows:

$$P_{total}= P_{dynamic}+P_{static}+P_{sc}$$

In CMOS circuits flip flop are the basic building blocks in digital electronic circuits and as well as in real time processing applications. Flip-Flop whichis an electronic circuit stores a logical state of more data inputsignals to a clock pulse response. Flip-flops are used in Computational circuits for the operation of a particular sequence during repeated clock intervals for receiving and maintaining data for a particular time period. During each falling and raising clock edge signal, the data stored in a flip-flop is available readily. So that it can be applied as input toother sequential and combinational Circuitry-Flipflop (Delay Flipflop) is an integral part for a sequential part of a digital system construction. To achieve low area and low power we have designed various D flip flop for analyzing the performance of D-flipflop with variousarchitectures with respect to performance metrics such as power, area and delay. Previous techniques are compared and summarized with the proposed technique presented in this paper.

2. Parameters for Power Gating

Additional considerations for timing closure implementation have to be taken for Power gating. The parameters needed to be considered and values chosencarefully for a successful implementation of themethodology are as following:

2.1 Power gate Size
2.2 Gate control slew rate
2.3 Simultaneous switching capacitance
2.4 Power gate leakage

2.1 Power gate Size

Selection of Power gate Sizeis to handle the amount of current switchingat any given time. The gate should be bigger such that there is no measurable voltage drop (IR) due to the gate. As a rule the size of the gate is selected to be approximately 3 times to the switching capacitance. Designers can choose between P-MOS (header) or N-MOS (footer) gates. Usually for the same switching current, a footer gate tends to be smaller in area. Analysis tools for Dynamic power can measure accurately the switching current and the size for the power gate is predicted.

2.2 Gate control slew rate

It is an important parameter which determines the power gating efficiency. Larger slew rate takes will take much time for switch off and switch on the circuit and so the efficiency of power gating will be affected. Controlling of slew rate is done by buffering the signal of the gate control.

2.3 Simultaneous switching capacitance

This is an important constraint which refers to the part of the circuit that can be simultaneously switched without network integrity getting affected. If a large part of the circuit is simultaneously switched, the power network integrity can be compromised by the resulting "rush current". The circuitis to be switched in stage in order to prevent this.

2.4 Power gate leakage

To maximize power savings one of the important consideration is leakage reduction because power gates are made of active transistors.

3. Existing Leakage Current Reduction Techniques Review

Different types of techniques are there to tackle leakage power. An efficient way is provided by each technique to reduce leakage power, the application of each technique is limited by its disadvantages. We here in this section reviews our proposed technique with previously proposed circuit techniques which includes Sleep techniques like Sleepy Stack, Dual Sleep, Dual Stack techniques for the reduction of sub threshold leakage power and comparison is done with respect area and power.

3.1 Sleep Technique

The most known technique is the sleep technique. In the sleep technique, a "sleep" PMOS transistor is placed between pull-up network and Vdd of the circuit and a "sleep" NMOS transistor is placed between the pull-down network and the ground as shown in the Figure 1. The circuit is turned off by the sleeptransistors by cutting off the power rails. When the circuit is active the sleep transistors are turned on and when the circuit is idle they are turned off. By the power source turning off the, this technique will effectively reduce the leakage power. However, after sleep mode output will be floating, so thetechnique results in state destruction and also a floating output voltage.

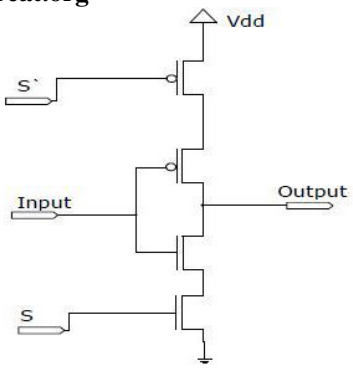

Figure 1: Sleep Technique

3.2 Stack Technique

Another technique to reduce the leakage power is the stack approach. In this a stack effect is forced on the transistor by dividing an existing transistor into two transistors as shown in Figure 2. So, that the divided transistors will increase delay significantly and could be a limit to the usefulness of this approach.

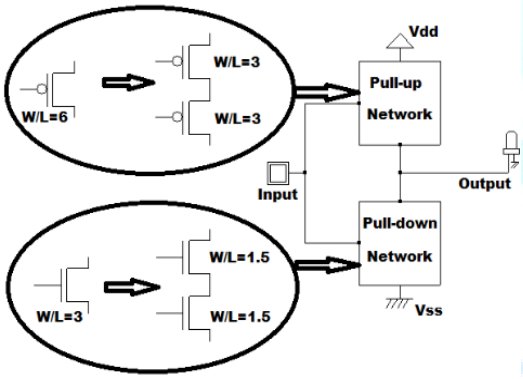

Figure 2: Stack Technique

3.3 Sleepy Stack Technique

The sleepy stack approach which is shown in Figure 3 combines the sleep and stack techniques. The stack technique divides existing transistors into two transistors like the stack approach and the sleep transistors are added in to one of the divided transistors parallelly. During sleep mode the sleep transistors are turned off and the leakage current is suppressed by the stacked transistors while saving state. Due to each sleep transistor which is placed in parallel the resistance of the path is reduced, to the one of the stacked transistors. So, in active mode delay is decreased. However, for this approach penalty of area is a significant matter since three transistors replaces every transistor and also additional wires are added for sleep signals S and S'.

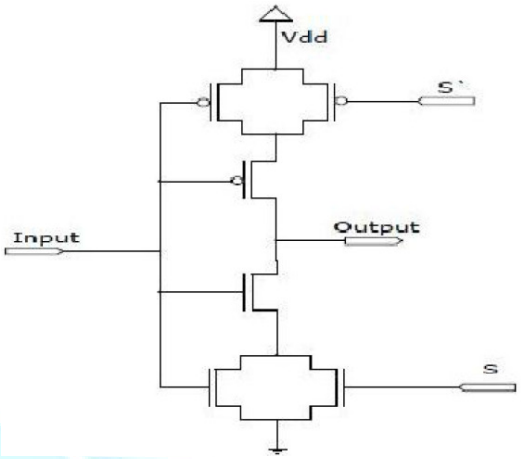

Figure 3: Sleepy stack Technique

3.4 Dual Sleep Technique

In dual sleep technique for each NMOS or PMOS block two sleep transistors are used as shown in Figure 4. In ON state one sleep transistor is used to turn on and the other in OFF state one is used to turn on. The advantage of the two extra pull-down , two extra pull-up, transistors in Dual sleep approach is used in sleep mode either in ON state or OFF state. It means that, it uses two pull-up and two pull-down sleep transistors. The pull down NMOStransistor is ON When S=1 and when the S'=0 the pull-up PMOS transistor is ON. So in ON state this arrangement will work as a normal device. S is forced to '0' During OFF state and so the NMOS transistor (pull down) is OFF and PMOS transistor is ON and the pull-up (PMOS) transistor is OFF while NMOS transistor is ON. So when a PMOS in series with an NMOS in OFF state both pull-up and pull-down circuit is likely to reduce power.

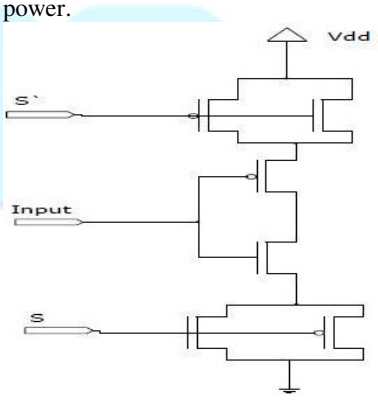

Figure 4: Dual Sleep Technique

3.5 Dual Stack Technique

In this technique two stacked sleep transistors are used in Vdd and two stacked sleep transistors in ground as shown in Figure 5. So, in this technique

leakage reductionoccurs in two ways. First, due to the stack effect of the sleep transistors and secondly due to the sleep transistor effect. We know pmos transistors are inefficient in passing ground; similarly nmos transistors are inefficient in passing V_{dd}. So, this stacked sleep technique uses a pmos transistor in Ground and in Vdd an nmos transistor during sleep mode for maintaining the exact logic state. During sleep mode for maintaining the logic state twoextra transistors are designed.

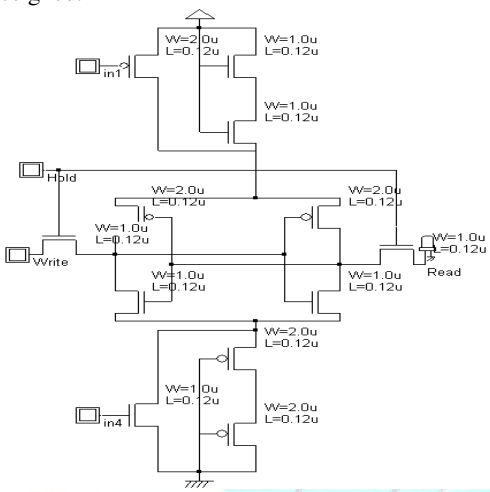

Figure 5: Dual Stack Technique

4. Proposed Leakage Current Reduction Technique

The Proposed power gating technique is as shown in figure 6.

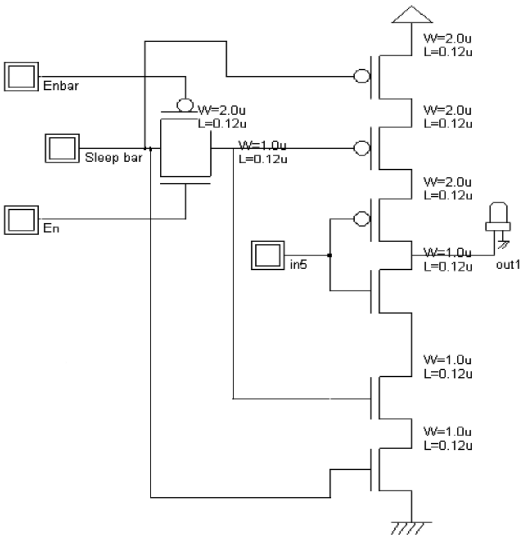

Figure 6: Proposed Technique

The Proposed Sleep Circuit has different modes of operation as shown below:

A. Active mode

B. Standby mode

C. Sleep to active mode transition

In active mode, the transistor sleep Signal is at logic' 1 ' and both the sleep transistors M2, M1 (Enbar and En Transistors from the top side) remain ON. In this case both the transistors will offer very low resistance and the V_{GND} (virtual ground) node potential is pulled down to the ground potential, which makes the logic difference between the logic circuit and virtual ground (VGND) node potential equal to the supply voltage approximately.

There are certain benefits in combining stacked sleep transistors. First the magnitude of the power supply fluctuations during sleep mode transitions will get reduced because this transition is gradual. Secondly, while in the sleep transistor conventional power gating technique uses a high threshold device for minimizing leakage, with a normal threshold device the same effect can be achieved using a stacked sleep structure.

Also in active mode, the sleep Signal to the transistor is at logic' 1 ' and the sleep transistors that is both the NMOS1 and NMOS2 (which are used for the purpose of sleep from the circuit bottom) remains ON and by giving logic 'O', the control transistor is OFF . In this case both the transistors offers very low resistance and the V_{GND} (virtual ground) node potential is pulled down to ground potential, making the logic difference to the logic circuitry approximately equal to the supply Voltage. And the leakage current is reduced by stacking effect, turning the transistors NMOS1 and NMOS2 OFF and vice versa for the header switch.

Positive potential at the intermediate node has the following effects

- Gate to source voltage for NMOS1 (VgNMOS1) will become negative.
- Negative body to source potential (Vdsl) NMOS1 decreases, resulting in the less drain induced barrier lowering.
- Drain to source potential (VdNMOS2) for NMOS2 is less comparing with NMOS1, because most of the voltage drops across the NMOS1 is in sleep mode.

This will reduce the drain barrier lowering significantly.The design analyzed gives major contribution for sleep to active mode in terms of sleepmode comparing with stacking power gating. Sleep mode occurs when circuit switches from sleep to active mode and vice versa. In first stage the sleep transistor (NMOS1) working as a diode on the control transistor M I which is connected across the drain and the gate of the sleep transistor (NMOS1). Due to the drain to source current of the sleep transistor drop in a quadratic manner. This reduces the voltage fluctuation on the ground

and power net andit also reduces the circuit wakeup time. So in sleep to active mode switching, we are turning ON transistor NMOS1 initially and after a small duration of time NMOS2 willbe turned ON to reduce the GBN. Control transistor in second stage is off that sleep transistor will work normally and during sleep to active mode switching, transistor NMOS1 will turned ON and transistor NMOS2 will turned ON after a small duration of time. Isolation is done for the logic circuit and the ground for a short duration as NMOS2 transistor is turned OFF. In this duration, the reduction of GBN can be greatly controlled by the intermediate node VGND2 voltage and operating the transistor NMOS2 in triode region. The intermediate node voltage (VGND2) can be controlled by Inserting proper amount of delay that is less than the discharging time of the NMOS1 transistor and with Proper selection of the capacitance C2. Leakage current will also be reduced by the stacking effect, turning both NMOS1 and NMOS2 sleep transistors OFF. This raises VGND2, the intermediate node voltage to positive values due to small drain current. Positive potential at the intermediate node has the following effects:

Gate to source voltage of NMOS1 (VgNMOS1) will become negative. Negative body to source potential (VbNMOS1) for NMOS1 causes body effect more. Drain to source potential (Vdsl) for NMOS1 decreases, which results in less drain induced barrier lowering.Drain to source potential (VdNMOS2) for NMOS2 is less when compared to NMOS1, because most of the voltage will drop across the NMOS1 in sleep mode. So, this reduces the drain induced barrier lowering significantly.

5. Area and Power Analysis

We used DSCH software for the logic design. Based on primitives, a hierarchical circuit will be builted and simulated.

Micro wind is a tool at layout level which is used for designing and simulating circuits. The tool features full editing facilities like copy, cut, past, duplicate, move, etc., various views like MOS characteristics, 2D cross section, 3D process viewer, and also an analog simulator. The Microwind program allows the designing and simulating of an integrated circuit at physical description level. The Experimental Methodology is as shown in Figure7.

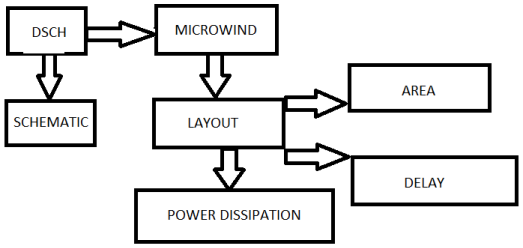

Figure 7: Experimental Methodology

So, here after the schematic design using DSCH the circuit is tested for evaluation. Then Verilog code is generated in DSCH which is then complied.

In this paper we estimatethe power dissipation for five design techniques.

5.1 Simple Flipflop

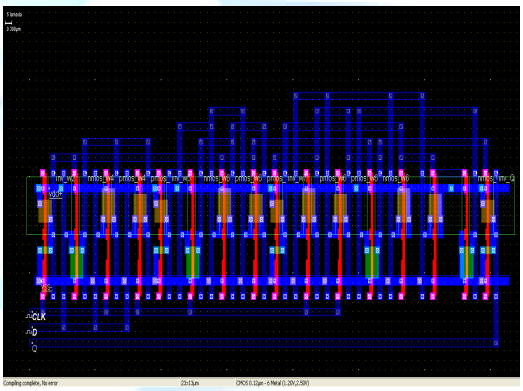

Figure 8: Layout of simple flip flop

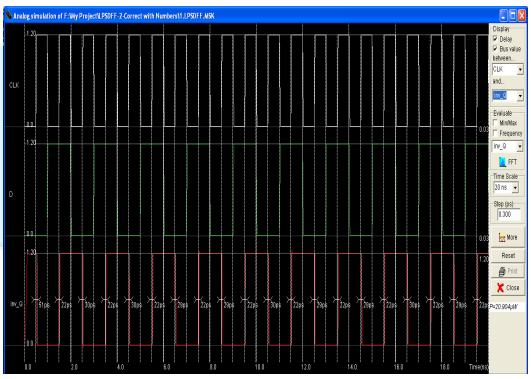

Figure 8: Power Analysis of simple flip flop

5.2 Sleepy Stack

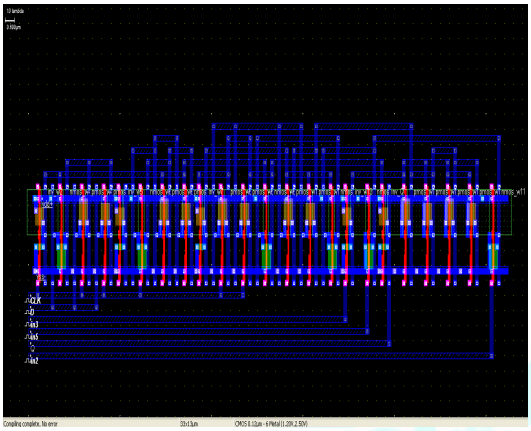

Figure 9: Layout of Sleepy Stack

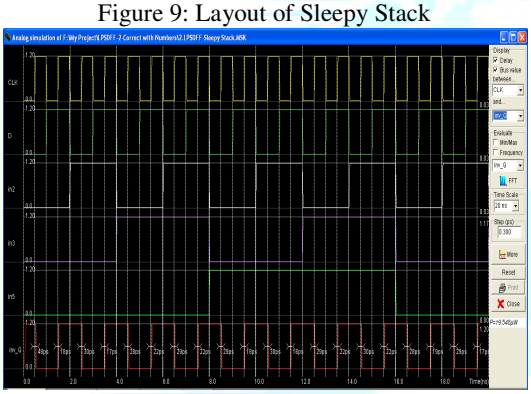

Figure 10: Power Analysis of Sleepy Stack

5.3 Dual Sleep

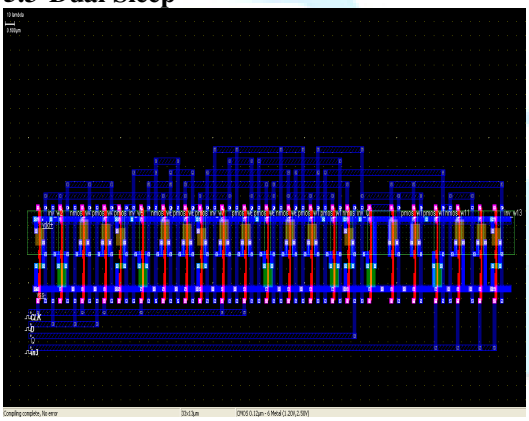

Figure 11: Layout of Dual Sleep

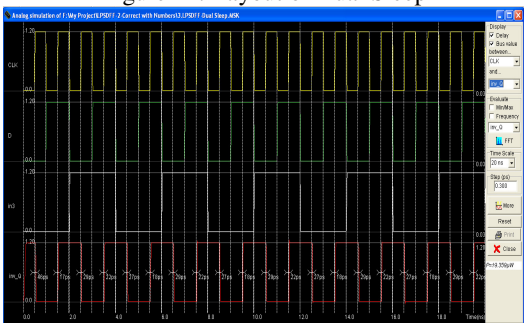

Figure 12: Power Analysis of Dual Sleep

5.4 Dual Stack

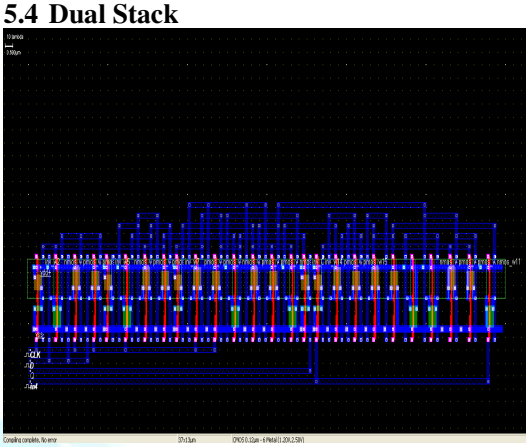

Figure 13: Layout of Dual Stack

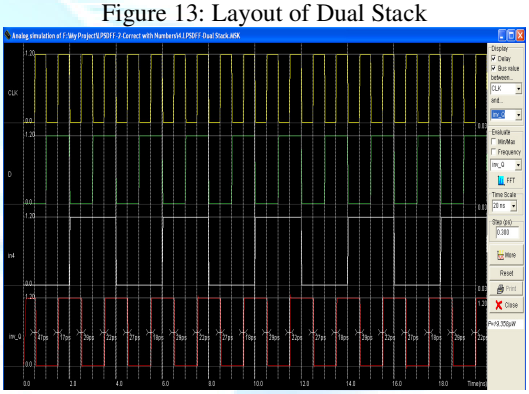

Figure 14: Power Analysis of Dual Stack

5.5 Proposed Technique

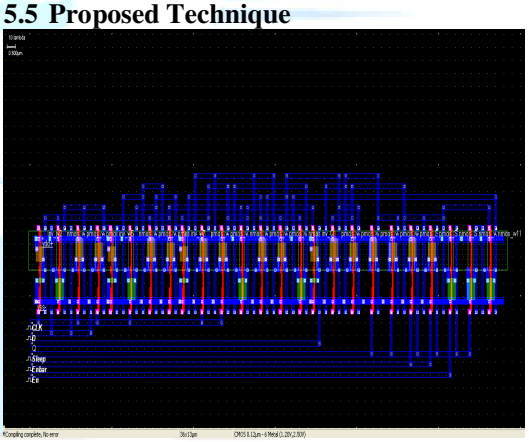

Figure 15: Layout of Proposed Technique

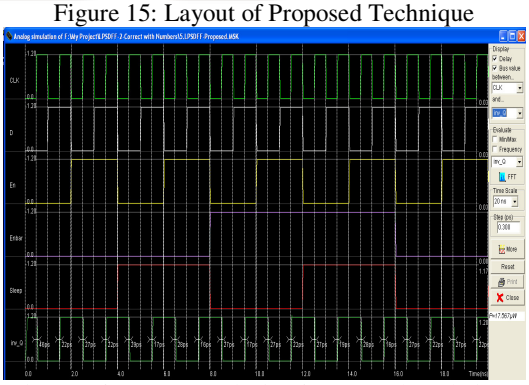

Figure 16: Power Analysis of Proposed Technique

S.No	Method	Area	Power
1	SimpleFlipflop	23x13 µm	20.904µW
2	Sleepy Stack	33x13 µm	19.548 µW
3	Dual Sleep	33x13 µm	19.359 µW
4	Dual Stack	37x13 µm	19.358 µW
5	Proposed	36x13 µm	17.567µW

6. Conclusion

In CMOS technology, consumption of sub threshold leakage power is a greatchallenge. Although previous techniques are effective, no perfect solution for the reduction of the leakage power consumption is known. Therefore, a designer chooses techniques based upon the design criteria and technology. In this paper, we provide a new circuit structure for dual stack which is the new remedy for the designer in terms of the static and dynamic powers. The dual stack technique will retain the original state unlike the sleep transistor technique. The dual stack approach will show the least speed power product among all the methods.Therefore, this technique provides ultra-low leakage power consumption for designers who require with much lessspeed power product. So, this can be used for the future integrated circuits for Area & Power Efficiency.

REFERENCES

[1] Powell M, Yang SH, Falsafi B, Roy K, Vijay Kumar TN. Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep submicron. Proc. of the International Symposium on Low Power Electronics & Design, July 2000; 90-95.

[2] Park JC, Mooney VJ, Pfeiffenberger P. Sleepy Stack Reduction of Leakage Power. Proc. of the International Workshop on Power and Timing Modeling, simulation and Optimization, September 2004; 148-158.

[3] Park J. Sleepy Stack: a New Approach for Low Power VLSI design and Memory, Ph.D., School of ECE, Georgia Inst. of Technology, 2005.

[4] Mutoh S, Douse Ki T, Matsuya Y, Aoki T, Shigemitsu S, Yamada J. Power Supply High-speed Digital Circuit Technology with Multi threshold Voltage CMOS. IEEE Journal of Solis State Circuits 1995; 30(8): 847–854.

[5] Kim N, Austin T, Beau D, Madge T, Flaunters K, Hu J, Irwin M, Kinder V, Narayanan V. Leakage Current: Moore's Law Meets Static Power. IEEE Computer 2003; 36: 68–75.

[6] Min KS, Kawaguchi H, and Sakurai T. Zigzag Super Cut-off CMOS (ZSCCMOS) Block Activation with Self-Adaptive Voltage Level Controller, An Alternative to Clock-gating Scheme in Leakage.

[7] Shin J, Kim T. Technique for transition energy-aware dynamic voltage assignment. IEEE Trans. Integr. Circuits Syst. Exp. Briefs 2006; 53(9): 956–960.

[8] Chaos W, Kim T. Optimal voltage allocation techniques for dynamically variable voltage processors. ACMTrans. Embedded Comput. Stys 2005; 4(1): 211–230.

[9] Ishihara T, Acura H. Voltage scheduling problem for dynamically variable voltage processors. Proc.IEEE/ACM Int. Seem. Low Power Electron. Des.1998; 197–202.

[10] Fallow F, Pedal M. Standby and active leakage current control and minimization CMOS VLSI circuits.IEICE Trans. Electron 2005; E88-C (4): 509–519.

[11] Friedrich J et al. Design of the Power6 microprocessor. Proc. IEEE/ACM Int. Solid-State Circuits Conf., Feb. 2007; 96–97.

BIOGRAPHIES

Mr. KODALI VENKATA BHANU PRAKASH born in Gudur, Nellore Dist., AP., is M.Tech (VLSI) student from PBR VITS, Kavali, Department of ECE, JNTUA. He obtained his B.Tech from NBKR Institute of Science and Technology (NBKRIST), Vidyanagar, AP. His interesting fields are Core VLSI; Low power Chip Design, Analog VLSI.

Ms. M.PAVITRA is working as Associate Professor in ECE Dept. PBR VITS, Kavali. She has been guiding U.G. &P.G. projects since six years in this institution. She also presented papers in several international journals and international conferences. Her interesting Fields are Core VLSI, Analog & Digital VLSI, Embedded Systems and Testability Issues